

MK0160VP LDMOS TRANSISTOR

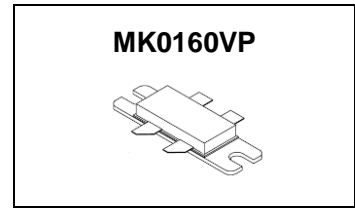
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Preliminary Datasheet V1.0

550W, 50V High Power RF LDMOS FETs

Description

The MK0160VP is a 550-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.2 GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.



Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c=85^\circ\text{C}$, $P_{out}=500\text{W CW}$,	$R_{\theta JC}$	TBD	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

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Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

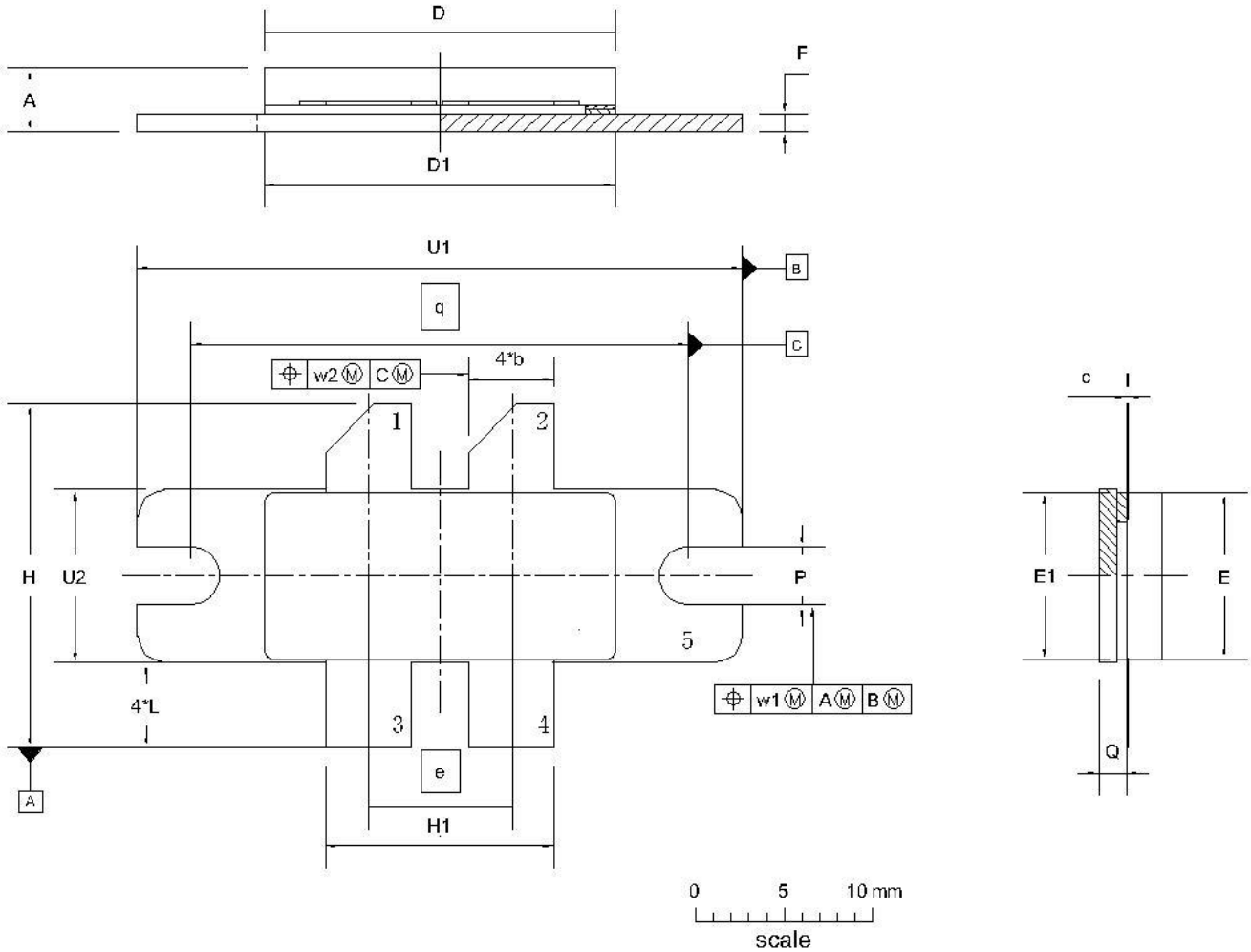
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V _{GS} =0, I _{DS} =1.0mA	V _{(BR)DSS}		128		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 50V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Gate—Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{GSS}	—	—	1	μA
Gate Threshold Voltage (V _{DS} = 50V, I _D = 600 μA)	V _{GS(th)}	—	2.62	—	V
Gate Quiescent Voltage (V _{DD} = 50 V, I _D = 100 mA, Measured in Functional Test)	V _{GS(Q)}	—	3.3	—	V
Drain source on state resistance (V _{DS} = 0.1V, V _{GS} = 10 V) Each section side of device measured	R _{ds(on)}		217		mΩ
Common Source Input Capacitance (V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz) Each section side of device measured	C _{ISS}		208		pF
Common Source Output Capacitance (V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz) Each section side of device measured	C _{OSS}		49.6		pF
Common Source Feedback Capacitance (V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz) Each section side of device measured	C _{RSS}		1.14		pF

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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



UNIT	A	b	C	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂
mm	4.72	3.94	0.15	20.02	19.96	8.89	9.50	9.53	1.14	19.94	12.83	5.33	3.38	1.70	27.94	34.16	9.91	0.25	0.51
	3.43	3.68	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.57	4.32	3.12	1.45		33.91	9.65		
inches	0.186	0.155	0.006	0.788	0.786	0.35	0.374	0.375	0.045	0.785	0.505	0.210	0.133	0.067	1.100	1.345	0.390	0.01	0.02
	0.135	0.145	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.495	0.170	0.123	0.057		1.335	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/6/27	Rev 1.0	Preliminary Datasheet Creation

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